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REISSUE PATENT APPLICATION TRANSMITTAL

Address to:

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Attorney Docket No.	042390.P3275R
First Named Inventor	A. Ira Horden
Original Patent Number	5,812,860
Original Patent Issue Date (Month/Day/Year)	09/22/1998
Express Mail Label No.	EL034436815US

APPLICATION FOR REISSUE OF: (check applicable box) ☒ Utility Patent ☐ Design Patent ☐ Plant Patent

APPLICATION ELEMENTS

1. ☒ *Fee Transmittal Form *(PTO/SB/56)* *(Submit an original, and a duplicate for fee processing)*
2. ☒ Specification and Claims *(amended, if appropriate)*
3. ☒ Drawing(s) *(35 U.S.C. 113)*
4. ☒ Reissue Oath / Declaration (original or copy) *(37 C.F.R. § 1.175)(PTO/SB/51 or 52)*
5. Original U.S. Patent
   ☒ Offer to Surrender Original Patent *(37 C.F.R § 1.178)* *(PTO/SB/53 or PTO/SB/54)*
   or
   ☐ Ribboned Original Patent Grant
   ☐ Affidavit / Declaration of Loss *(PTO/SB/55)*
6. ☒ Original U.S. Patent currently assigned?
   ☒ Yes ☐ No
   (If Yes, check applicable box(es))
   ☒ Written Consent of all Assignees *(PTO/SB/53 or 54)*
   ☐ 37 C.F.R. § 3.73(b) Statement ☐ Power of Attorney

ACCOMPANYING APPLICATION PARTS

7. ☐ Foreign Priority Claim *(35 USC 119)* *(if applicable)*
8. ☐ Information Disclosure Statement (IDS)/PTO - 1449 ☐ Copies of IDS Citations
9. ☐ English Translation of Reissue Oath/Declaration *(if applicable)*
10. ☐ *Small Entity Statement(s) *(PTO/SB/09-12)* ☐ Statement filed in prior application, Status still proper and desired
11. ☒ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. ☐ Other: .....

*NOTE FOR ITEMS 1 & 10: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

14. CORRESPONDENCE ADDRESS

☐ Customer Number or Bar Code Label (Insert Customer No. or Attach bar code label here) or ☒ Correspondence address below

Name	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP				
Address	12400 Wilshire Boulevard, Seventh Floor				
City	Los Angeles	State	California	Zip Code	90025
Country	U.S.A.	Telephone	(503) 684-6200	Fax	(503) 684-3245

Name (Print/Type)	Donna Jo Coningsby, Reg. No. 41,684		
Signature	Donna Jo Coningsby	Date	09/22/00

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09/22/00 JC813 U.S. PTO

FEE TRANSMITTAL for FY 1999

Patent fees are subject to annual revision.
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.
See 37 C.F.R §§ 1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT ($) 1,020.00

Complete if Known	
Application Number	
Filing Date	September 22, 2000
First Named Inventor	A. Ira Horden
Examiner Name	R. Sheikh
Group/Art Unit	unknown
Attorney Docket Number	042390.P3275R

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees to:
2. ☒ The Commissioner is hereby authorized to credit any over payments to:

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

☒ Charge Any Additional Fees Required Under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.

2. ☒ Payment Enclosed:
☒ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	21	- 20 =	1	X	18.00	=	$18.00
Independent Claims	7	- 3 =	4	X	78.00	=	$312.00
Multiple Dependent						=	

***or number previously paid, if greater, For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple Dependent claim, if not paid
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 330.00

FEE CALCULATION (continued)

3. ADDITIONAL FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	*Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	*Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	380	216	190	Extension for response within second month	
117	870	217	435	Extension for response within third month	
118	1,210	218	680	Extension for response within fourth month	
128	1,850	228	925	Extension for response within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	
Other fee (specify)				Reissue filing fee	690.00
Other fee (specify)					

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 690.00

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	Donna Jo Coningsby			Reg. Number	41,684
Signature	Donna Jo Coningsby	Date	09/22/00	Deposit Account User ID	02-2666

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Express Mail Label No. EL034436815US

PATENT APPLICATION

042390.P3275

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	)	September 21, 2000
Horden et al.	)	
Original Patent Number: 5,812,860	)	Group Art Unit: unknown
Issued: September 22, 1998	)	Examiner: R. Sheikh

For: **METHOD AND APPARATUS PROVIDING MULTIPLE VOLTAGES AND FREQUENCIES SELECTABLE BASED ON REAL TIME CRITERIA TO CONTROL POWER CONSUMPTION**

EL034436815US

"Express Mail" Label Number

9/22/00

Date of Deposit

I HEREBY CERTIFY THAT THE ENCLOSED PETITION IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED ABOVE AND IS ADDRESSED TO THE ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

Mark W. Bauaher

Name of Person Mailing Paper or Fee

Signature

PRELIMINARY AMENDMENT FOR REISSUE APPLICATION, OFFER TO SURRENDER THE ORIGINAL PATENT, AND ASSENT OF ASSIGNEE TO REISSUE

HONORABLE ASSISTANT COMMISSIONER FOR PATENTS,
Washington, D.C. 20231

SIR:

In accordance with 35 U.S.C. § 251, Applicant is hereby filing a reissue application with claims that are broader than those issued in the original patent.

Please enter the following amendment prior to examination so that there is a total of seven (7) independent and a total of twenty-one (21) claims pending in the application.

PATENT APPLICATION

042390.P3275

AMENDMENT

Amendment to Claims

Please add the following claims as shown below.

7. (Newly added) An apparatus, comprising:

a static random access memory;

a processor coupled to the static random access memory;

a voltage regulator adapted to provide at least two voltage potential levels to at least a portion of the processor; and

wherein the processor is adapted to adjust the voltage potential level provided by the voltage regulator depending on the operational load of the processor.

8 (Newly added) The apparatus of claim 7, wherein the voltage regulator is adapted to provide an idle voltage potential level and a peak voltage level.

9. (Newly added) The apparatus of claim 7, further comprising a state machine adapted to determine the operational load of the processor.

10 (Newly added) The apparatus of claim 9, wherein the state machine is further adapted to determine a minimum voltage potential level at which the processor can operate.

11 (Newly added) The apparatus of claim 7, further comprising a clock signal generator adapted to provide a clock signal of at least two frequencies.

12. (Newly added) A method comprising:

determining an instruction mix of a processor;

determining a frequency at which the processor may operate given the instruction mix; and

determining a voltage potential level corresponding to the frequency; and

providing at least a portion of a processor with the frequency and voltage potential level.

13. (Newly added) The method of claim 12, further comprising changing the frequency and voltage potential level in response to a change in the instruction mix of the processor.

14. (Newly added) A method of operating a processor, comprising:

adjusting the voltage potential level provided to at least a portion of the processor based on the instruction mix executed by the processor.

15. (Newly added) The method of claim 14, further comprising determining an operational frequency based on the instruction mix executed by the processor.

16. (Newly added) The method of claim 15, further comprising adjusting the operational frequency after adjusting the voltage potential level.

17. (Newly added) An article comprising: a storage medium having stored thereon instructions, that, when executed by a computing platform, results in:

adjusting the voltage potential level provided to at least a portion of the computing platform based on the instruction mix executed by the computing platform.

18. (Newly added) The article of claim 17, wherein the instructions, when executed, further result in determining a preferred operational frequency based on the instruction mix executed by the computing platform.

19. (Newly added) The article of claim 17, wherein the instructions, when executed, further result in computing platform executing the instruction mix at peak performance.

20. (Newly added) The article of claim 17, wherein the article further comprises a static random access memory device and the computing platform is coupled to the static random access memory.

21. (Newly added) The article of claim 20, wherein the static random access memory is adapted to store the instructions to be executed by the computing platform.

Remarks

Applicant hereby requests that United States Patent and Trademark Office initiate broadening reissue proceedings for the above-mentioned issued patent. Applicant requests that the preceding claims be added prior to examination.

Specification

A copy of the original patent is filed concurrently with this application. The copy of the original patent was prepared by transcribing the copy of the original application as filed on February 12, 1996. In addition, the text of the enclosed application has been modified, as required by 37 CFR § 1.173, to reflect the changes made by the amendment filed on September 26, 1997 and the amendment filed on January 28, 1998. These amendments have been shown as normal text as they appear in the original patent. No new matter has been added.

Oath and Declaration

Applicant has filed concurrently with this reissue application an oath and declaration that is believed to meet the requirements of 37 CFR §1.175.

Offer to Surrender the Original Patent

Patent No. 5,812,860 granted to Horden et al. on September 22, 1998 of which Intel Corporation, now sole owner by assignment, and on whose behalf and with whose assent the accompanying application is made, hereby offers to surrender said letter patent.

Assent of Assignee to Reissue

The undersigned assignee hereby avers in accordance with 37 CFR §3.73 that he is authorized to act on behalf of the assignees of the entire interest in the above-mentioned letters patent and hereby assents to the accompanying application.

Drawings for the Reissue Application

In accordance with M.P.E.P. §1413, Applicant hereby requests transfer of the drawings from the file of the original patent in lieu of new drawings. Applicant is enclosing with this reissue application a photocopy of the drawings of the patent as temporary drawings as permitted by 37 CFR § 1.174.

PATENT APPLICATION

042390.P3275

Request for Abstract of Title Report

Applicant is filing herewith a request for a certified Abstract of Title report and appropriate fee in accordance with 37 CFR § 1.171.

Support for Amendments.

As indicated above, claims 7-21 have been added. Support for the amendments is at least shown by the examples in FIG. 1 and described in Applicant's specification at column 3, line 9, through column 4, line 54.

Applicant respectfully submits that no new matter has been added.

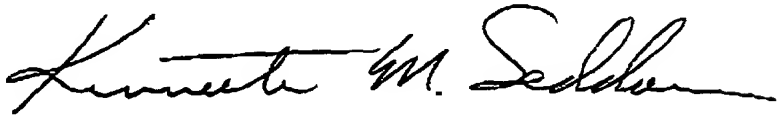
Conclusion

Applicant respectfully requests that the Examiner allow all pending claims.

Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666.

If the Examiner believes that there are any informalities which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (480) 554-9732 is respectfully solicited.

Respectfully submitted,
Ira Horden et al.



Kenneth M. Seddon
Patent Attorney
Reg. No. 43,105

Dated: 9-22-00

c/o Blakely, Sokoloff, Taylor & Zafman, LLP
12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA 90025-1026
(503) 264-0967

Our Ref.: 42390.P3275

UNITED STATES PATENT APPLICATION

FOR

A METHOD AND APPARATUS PROVIDING MULTIPLE VOLTAGES AND FREQUENCIES SELECTABLE BASED ON REAL TIME CRITERIA TO CONTROL POWER CONSUMPTION

Inventors: A. Ira Horden
Steven D. Gorman
Lionel S. Smith

Prepared By:

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EL034436815US

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to reducing power consumption by VLSI circuitry. More specifically, the invention relates to manipulating a voltage and a frequency supplied to VLSI circuitry to achieve lower average power consumption by the VLSI logic circuitry.

(2) Related Art

As more systems become portable, increased reliance will necessarily be placed on portable power supplies, particularly batteries. Reducing power consumption by processors becomes increasingly important as the industry moves to maximize battery life. Even in stationary systems, excessive power consumption translates into higher operational costs. Additionally, increasingly stringent governmental requirements and environmental standards militate toward reducing the power consumed in a computer system where possible.

The power consumed by CMOS VLSI circuitry is proportional to $f \times V^2$ where f is the frequency and V is the voltage. It is relatively common for power sensitive products to adjust the frequency to achieve a linear reduction in power consumption by the circuitry. Early processor packaging provided only a single set of voltage input pins (Vcc). Because external logic typically requires three or five volts, it has not been possible to separably adjust the voltage to achieve any power savings. VLSI fabrication techniques allow the introduction of two sets of power pins and accordingly two different voltage levels on a single chip. For example, a processor core is typically constructed on the die and surrounded by peripherals, all of which operate on the voltage of the processor core. Around these components is a lead frame which provides for connection to external devices. Each interface at the lead frame is known as a pad, and all the pads taken together are a pad ring. The pad ring is typically supplied by a separate

power supply. Different power supplies allow for improved noise characteristics and the use of different voltages as pad and core voltages. While this allows a separate core voltage and, therefore, some effect on the VLSI circuits power consumption, the VLSI circuits power consumption is still limited by the worst case application mix if the peak level of performance is to be maintained. For example, of a processor must operate at 32 MHz, the voltage maintained must allow operation at 32 MHz, e.g., must be $\geq$ 2.75 V.

Each frequency has a minimum voltage at which the CPU can operate and maintain operation. The required voltage normally increases with increased frequency. Frequency is a key measure of performances. Processors having greater peak performance require higher frequencies which depend in turn upon higher voltages with a significantly higher power consumption. While in most cases sufficient processing can be performed at lower frequencies, the performance rating of the processor relies on its ability to handle a worst case load. Thus, the voltage at which the CPU can operate at the frequency required for a worst case application mix is typically employed to insure performance does not degrade below the specified peak. This results in excessive power usage any time the processing capacity is not fully utilized.

It would be desirable to be able to maintain a high peak performance rating while reducing power consumption through use of lower voltages when peak processing is unnecessary. It would, therefore, be desirable to be able to adjust voltage and frequency based on a current application mix.

BRIEF SUMMARY OF THE INVENTION

A method and system for reducing poser consumption in VLSI circuit is disclosed. A state machine is used to coordinate a frequency from a clock signal generator with a voltage from a voltage regulator which is sufficient to allow a desired level of operation of the VLSI circuit at that frequency. Both the clock signal generator and the voltage regulator must be able to generate at least two frequencies or voltages, respectively. A level of VLSI circuit performance need is tracked, and the optimal frequency/ voltage pair that will allow the VLSI logic to run with a minimum power consumption. The level of VLSI circuit performance need is monitored either periodically or continually such that a new frequency / voltage pair can be dynamically selected as the desired level of operation changes. This allows the VLSI circuit to satisfy even a worst case application mix at an established peak rating maintaining a high performance rating while dramatically reducing power consumption over prior art systems.

In an alternate embodiment, a maximum power consumption level is established below the maximum performance level of the system. The system then selects the frequency / voltage pair which most closely meets the application mix need, but is still below the maximum power consumption allowed. This embodiment may be useful where a user is willing to forego some performance to ensure at least a certain level of battery life.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of one embodiment of the invention.

Figure 2a is a graph of power consumption at various frequency and voltage levels.

Figure 2b is a graph showing possible power saving over a fixed voltage system.

Figure 2c is a table of data from which Figures 2a and 2b are derived.

DETAILED DESCRIPTION OF THE INVENTION

A method and apparatus for reducing power consumption in VLSI circuitry are disclosed. In the following description, for purposes of explanation, specific applications, numbers, materials, and configurations are set forth in order to provided a full understanding of the present invention. However, it would be apparent to one skilled in the art that the present invention may be practiced without the specific details. In other instances, well-known systems are shown in diagrammatical or block diagram form in order not to obscure the present invention unnecessarily. The following description is written using a processor core. For the sake of illustration, it should be understood that the invention is also applicable to other VLSI logic devices including without limitation VGA chip sets, MPEG decoder devices, etc.

Figure 1 shows a block diagram of a system employing the invention. A processor core 1 running an operating system 4 and peripherals 17 coupled to a pad ring 16 is connected to a memory 3 by a bus 2. A power supply 7 which can be a battery or any other conventional power supply provides power to voltage regulator 5 which in turn provides a core voltage Vcc_{core} 9. The peripherals 17 typically operate on Vcc_{core} 9 and may include interrupt controllers and any other peripheral circuit packaged with the processor core. A second voltage Vcc_{pad} 10 is provided to the pad ring 16 within which the core 1 resides. The voltage regulator 5, clock generator 8, and state machine 6 are shown discretely. It is envisioned that any or all of these components may be incorporated on a single chip and such is within the scope contemplation of the invention.

Operating system 4 provides a control signal 15 to state machine 6. State machine 6 provides control signals 12 and 13 to voltage regulator 5 and clock generator 8, respectively. IN the current invention, it is anticipated that voltage regulator 5 will support at least two voltages, and clock generator 8 will support at least two frequencies. The voltage regulator 5 is envisioned

to include both the case where a single voltage regulator provides all supported voltages and the case where multiple voltage regulators provided different voltages. In the second case, changing the voltage supplied entails switching between independent voltage regulators. Both arrangements are commercially available. Similarly, clock generator 8 can produce its multiple frequencies using different crystals, clock division, or any other conventional way. Clock generator 8 responds to control signal 13 for providing a clock signal 14 to the state machine 6. The state machine 6 synchronizes the incoming clock signal 14 to the state machine 6. The state machine 6 synchronizes the incoming clock signal 14 to the voltage change and provides synchronized clock signal 11 to the core processor 1. Voltage regulator 5 provides one of its supported voltages as the Vcc_{core} 9 responsive to the control signal 12 from state machine 6. State machine 6 must insure that the specification of the processor core is continually adhered to. To this end, state machine 6 must control the slew rate of the voltage at the transition point, maintaining the appropriate slew for the particular device.

In one exemplary embodiment, voltage regulator 5 supports two voltages, and clock generator 8 supports two frequencies. One frequency corresponds to peak performance, for example, 32 MHz, and a second frequency corresponding to an idle core frequency, for example, 16 MHz. Voltage regulator 5 is configured to provide the minimum voltages required to operate the processor at 16 and 32 MHz which the clock generator 8 could supply. State machine 6 through control signals 12 and 13 insures that the voltage regulator 5 supplies the idle voltage when clock generator 8 is supplying an idle frequency, and the voltage generator 5 supplies a peak voltage when the clock generator 8 is supplying a peak frequency.

Operating system 4 notifies state machine 15 whether the core should be operating at peak or idle frequencies and voltages. In this embodiment, the operating system 4 need only

identify whether core utilization and the corresponding required throughput can be handled at the supported idle frequency or if a higher frequency is required. If the state machine is in idle state and a higher frequency is required, the O/S asserts a switch state signal along control line 15. The state machine 6 then uses control lines 13 and 14 to drive the voltage regulator 5 and the clock generator 8 into the peak state. Conversely, if the total core usage could be accommodated at the idle state and the state machine is in the idle state, the O/S need not signal the state machine at all. An analogous case exists for transitioning the state machine from idle to peak. In an alternate embodiment, this time functionality may be performed using a hardware switch (not shown) (or even second state machine) to provide input to the state machine.

It will be recognized by one of ordinary skill in the art that even this two voltage embodiment will achieve significant power savings. In the above example, if the idle voltage is 2 V and the peak voltage is 2.75V, and if we assume an even distribution between idle and peak performance, power consumption is reduced by 36% over a platform having a single peak voltage and a single frequency. Moreover, a power saving of 16% is achieved over a system having a single peak voltage of 2.75, but a variable frequency. As a practical matter, real systems tend to spend greater than 50% of their time in an idle mode, so reduction in power consumption can be expected to be even greater than the above example.

In an alternate embodiment, a voltage regulator 5 supports any number of voltages up to a continuum between two end points. It is envisioned that supporting a plurality of voltage pairs corresponding to different peak and idle levels will be a common form of this embodiment. Similarly, the clock generator 8 supports a plurality of frequencies and will be recognized by one of ordinary skill in the art that by supporting a multitude of voltages and frequencies, the granularity of the power reduction system can be improved such that the power expended more

closely approximates the minimum power actually required to do the processing performed. In this embodiment, the operating system 4 acquires some objective measure of processor need for each application (not shown) seeking access to the processor core 1 which may or may be in MIPS, MFLOPS or another objective measure of processor need. One way this measure may be provided is by having each application tell the O/S its need or expected need based on operations to be performed. Modification to application programs which would be needed to provide this functionality would be readily apparent to persons skilled in the relevant art. The operating system 4 accumulates the processor need for all currently active applications. The operating system 4 then directs the state machine to transition into a state which as closely as possible matches the frequency and voltage to the application mix currently accessed in the processor core 1. It is envisioned that other considerations may in some cases drive voltage/ frequency pair selection. Among the other considerations are temperature, device behavior, and performance data.

In yet another embodiment, a maximum power consumption level is established by user, the operating system 4 or some sort of external consideration. This maximum power consumption basically creates a cap on the peak performance attainable. The operating system 4 creates a new peak at the closest supported frequency voltage point to the maximum power of consumption level. When this artificial peak is established, the system operates as it did in the embodiment discussed immediately above. Specifically, if the current application mix does not require the new peak performance level, the operating system drives the state machine into the lowest state which will meet the current mix requirements.

Figure 2a reveals the power consumption curves and various voltages and frequencies for a sample system. **Figure 2a** shows the maximum frequency which the sample system could

operate at 1.75V is 12MHz. At 2V, the system can operate up to 16 MHz, at 2.25V up to 20 MHz, at 2.5V up to 20 MHz, at 2.75 or 3V. The system can operate at least to 32 MHz. As the graph depicts, for any supported point, a lower voltage would yield a lower power of consumption at the same frequency. **Figure 2b** shows a graph of one embodiment of the invention, power usage at various frequencies. Prior art, the power consumption curve in 3V, the voltage is fixed at and the frequency is variable is also graphed in **Figure 2b**. This graph illustrates the power savings that can be achieved at any point in time by providing the ability to modify the voltage to the minimum required to operate at the desired frequency. The aggregate power saving over time will depend on the granularity, e.g. number of voltage levels supported and the amount of time spent operating at each frequency. **Figure 2c** shows the data from which Figures 2a and 2b are derived. While the graphs and data provide values up to 32MHz, it is anticipated that the invention is not so limited and could be extended to any processor frequency. Such is considered within the scope and contemplation of the invention.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will however be evident that various modifications and changes can be made thereto without departing from the broader spirit and scope of the invention.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will however be evident that various modifications and changes can be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense. Therefore, the scope of the invention should be limited only by the appended claims.

CLAIMS

What is claimed is:

1. A system comprising:

a processor coupled to memory by a bus, the processor having a processor core and a pad ring, the processor core having an independent power supply;

a voltage regulator providing a plurality of voltages and providing the independent power supply;

a clock signal generator providing a clock signal at a plurality of frequencies;

a state machine to coordinate voltage and clock frequency to the processor core; and

an operating system running on the processor, the operating system monitoring an application mix executing in the processor to determine a required frequency, and determining a minimum voltage at which the processor core can operate at the required frequency, wherein the operating system directs the state machine to enter a state in which the required frequency is supplied by the clock signal generator and a closest supported voltage equal to or greater than the minimum voltage is supplied by the voltage regulator.

2. The system of claim 1 wherein the voltage regulator provides one of an idle voltage of a peak voltage.

3. The system of claim 1 wherein the voltage regulator can provide one voltage corresponding to each frequency supported by the clock signal generator.

4. A method of reducing power consumption by a processor core and a pad ring comprising the steps of:

accepting a mesure of processor core performance need of each application currently seeking access to the processor core;

accumulating each measure of processor core performance need to find total current need:

calculating a minimum frequency that will allow the processor core to meet the total current need for the time period:

selecting a lowest supported frequency equal to or greater than the minimum frequency to be a required frequency:

finding a minimum supported voltage at which the processor core can operate at the required frequency independent of a voltage required by the pad ring;

supplying the required frequency and the minimum supported voltage to the processor core; and

dynamically changing the required frequency and the minimum supported voltage supplied responsive to a change in the current application mix.

5. A method of reducing power consumption by a processor core and a pad ring comprising the steps of:

establishing a maximum allowable power consumption;

finding a maximum supported frequency which will allow the processor core to remain below the maximum allowable power consumption at the minimum supported voltage;

selecting a required frequency to be less than or equal to the maximum supported frequency:

finding a minimum supported voltage at which the processor core can operate at the required frequency independent of a voltage required by the pad ring:

supplying the required frequency and the minimum supported voltage to the

processor core: and

dynamically changing the required frequency and the minimum supported voltage supplied responsive to a change in the current application mix.

6. The method of claim 5 wherein a required frequency less than the maximum supported frequency is selected whenever a total processor core performance need of the current application mix can be met by a lower supported frequency

ABSTRACT

A method and system for reducing power consumption in a processor core. A state machine used to coordinate a frequency from a clock signal generator with a voltage from a voltage regulator which is sufficient to allow operation of the processor at that frequency. Bot the clock signal generator and the voltage regulator must be able to generate at least two frequencies or voltages, respectively. A level of processor need is tracked and the lowest frequency/ voltage pair that will allow the processor core to satisfy the need is selected. The level of processor need is monitored either periodically or continually such that a new frequency / voltage pair can be dynamically selected as the application mix change

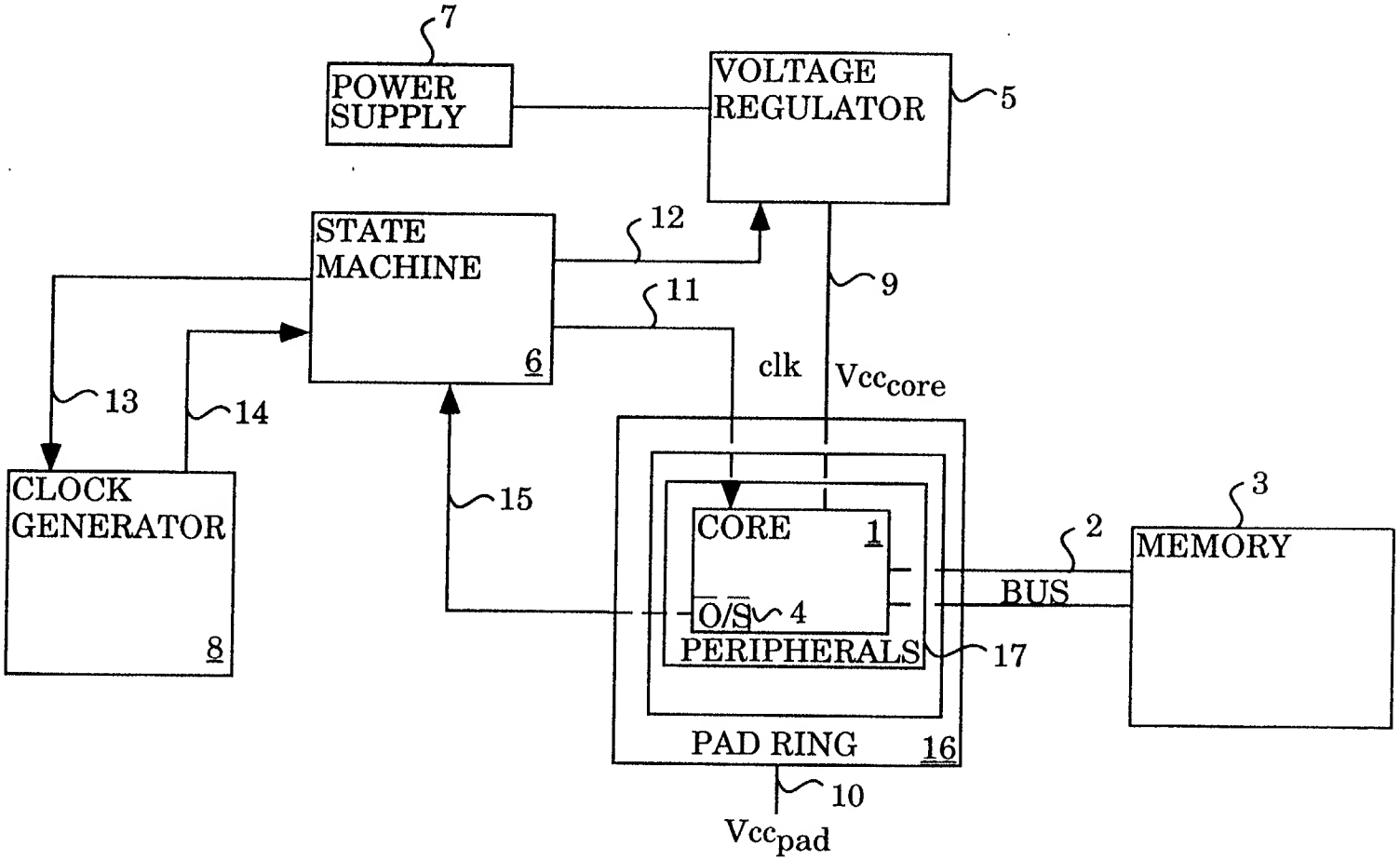
7
POWER SUPPLY
VOLTAGE REGULATOR
5
STATE MACHINE
6
12
11
9
clk
Vcc core
13
14
15
CLOCK GENERATOR
8
CORE
1
O/S
4
PERIPHERALS
17
2
BUS
3
MEMORY
PAD RING
16
10
Vcc pad

Fig. 1

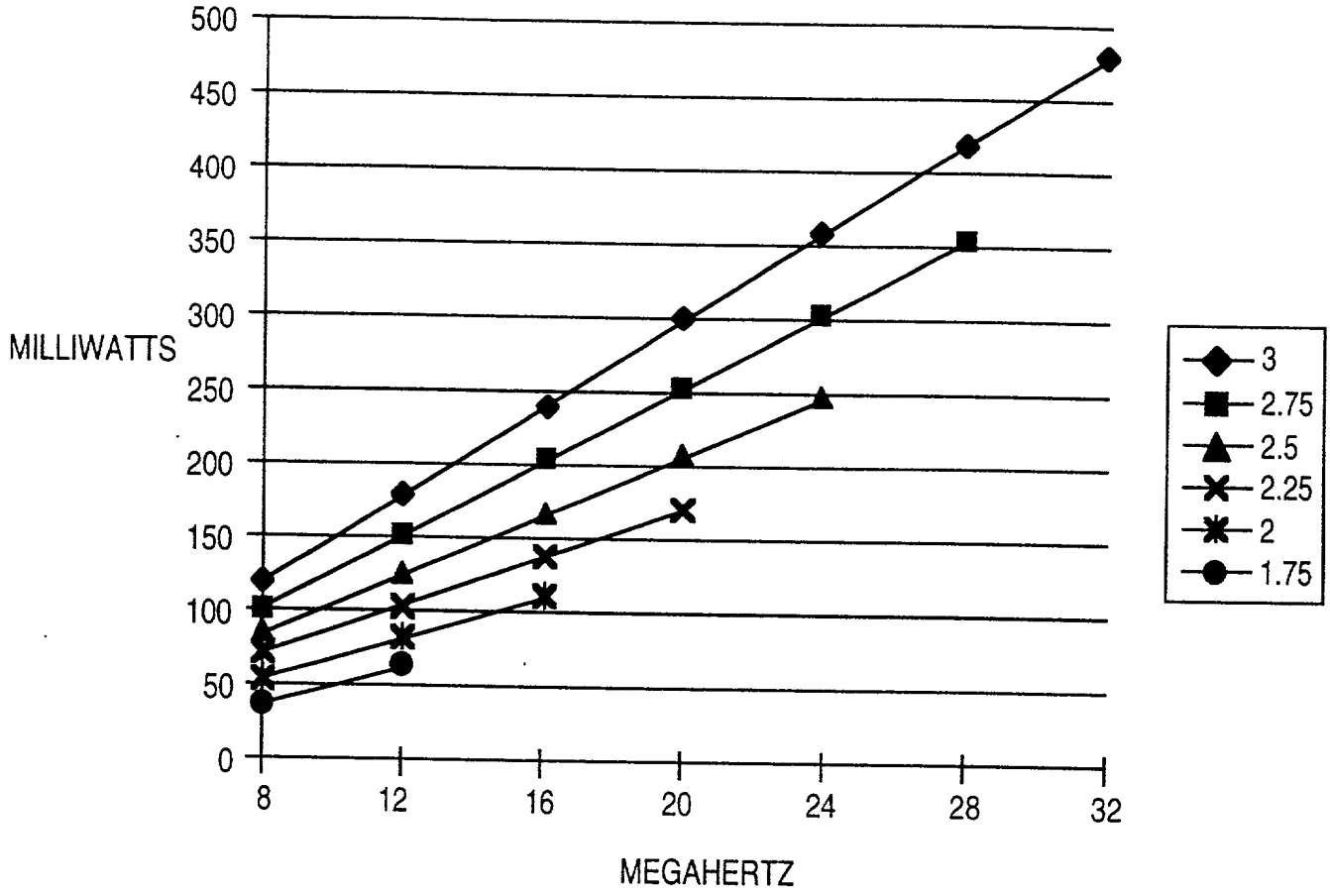
500
450
400
350
300
250
200
150
100
50
0
MILLIWATTS
8
12
16
20
24
28
32
MEGAHERTZ
3
2.75
2.5
2.25
2
1.75

Fig. 2a

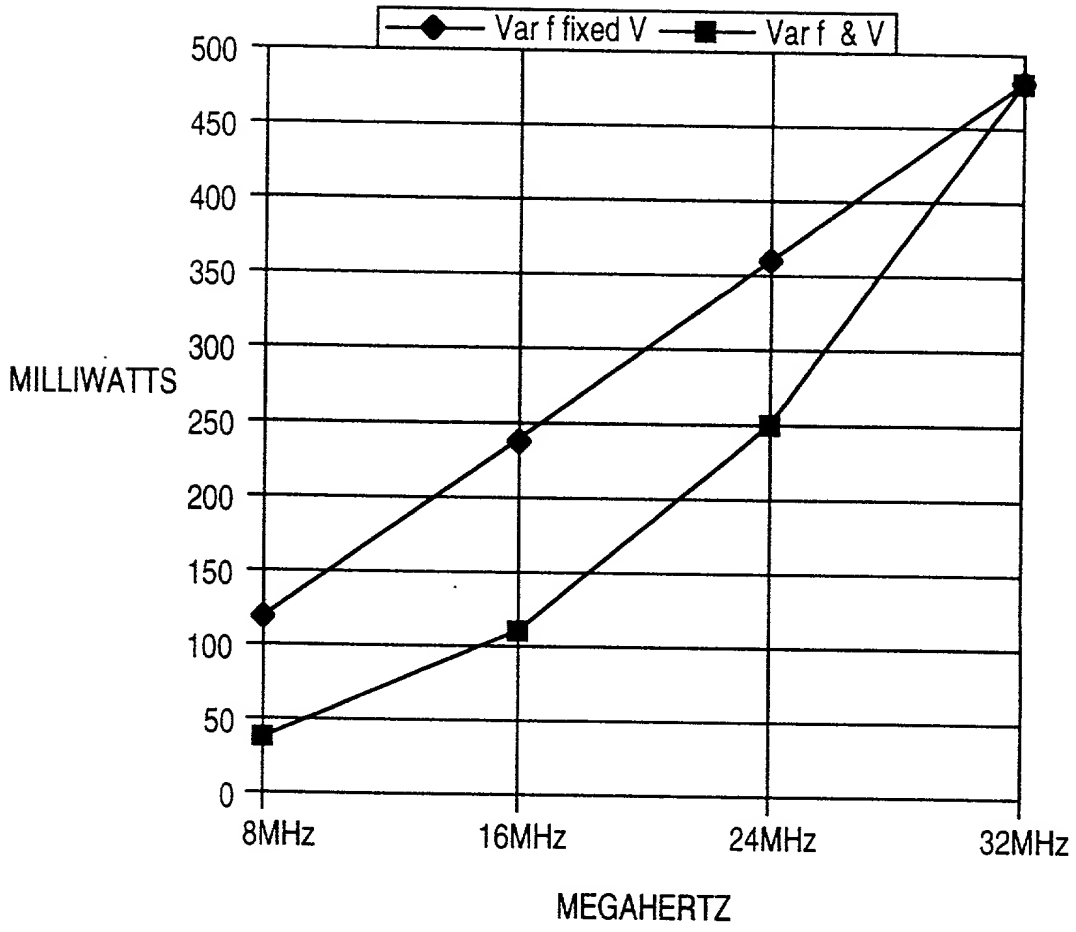
Var f fixed V
Var f & V
500
450
400
350
300
250
200
150
100
50
0
MILLIWATTS
8MHz
16MHz
24MHz
32MHz
MEGAHERTZ

Fig. 2b

MegaHertz

Vcc[V]	8	12	16	20	24	28	32
3	120	180	240	300	360	420	480
2.75	101	151	202	252	303	353	
2.5	83	125	167	208	250		
2.25	68	101	135	169			
2	53	80	107				
1.75	41	61					

Fig. 2c

Attorney's Docket No.: 42390.P3275R Patent

DECLARATION AND POWER OF ATTORNEY FOR REISSUE PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND APPARATUS PROVIDING MULTIPLE VOLTAGES AND FREQUENCIES SELECTABLE BASED ON REAL TIME CRITERIA TO CONTROL POWER CONSUMPTION

the specification of which is attached hereto and was issued as U.S. Patent No. 5,812,860 (the "original patent") from application number 599,648 filed February 12, 1996 (the "original application").

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to the original application, that the same was not in public use or on sale in the United States of America more than one year prior to the original application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of the original application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to the original application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States

provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

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Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells; Reg. No. P43,256, Peter Lam, Reg. No. P44,855; and Gene I. Su, Reg. No. 45,140; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

We verily believe the original patent to be wholly or partially inoperative:

by reason that the patent claims less than We had a right to claim in the patent. The claim or claims will be partly inoperative in failing to protect against infringement of all embodiments of our invention. Thus, We hereby indicate a desire to seek broadened claims as indicated in the Preliminary Amendment filed herewith. We also hereby affirm that this reissue application was filed diligently upon discovery of the following error.

The errors arose in the prosecution of the original application which resulted in the issuance of the patent. The attorney prosecuting the original application failed to appreciate the scope of the invention, and thus, limited the claims as indicated below.

The error arose without any deceptive intention on our part.

We further acknowledge my duty to disclose information which is material to the examination of the application under 37 CFR § 1.56.

Specifically, in claim 1, the clock signal generator need not have been recited.

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Inventor's Signature _____ Date _____

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Inventor's Signature ______________________ Date ______________

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Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.